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Waveform generator for electrical impedance tomography (EIT) using linear interpolation with multiplying D/A converters

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This paper describes the implementation of a multiplying digital-to-analogue (D/A) converter as a programmable waveform generator to be used in an electrical impedance tomography (EIT) system. Different digital techniques of generation waveforms are considered and the advantages and disadvantages of the chosen slope-plus-pedestal technique are presented. A wire-wrapped prototype system has been designed, and from measured frequency spectra the total harmonic distortion can be calculated to values between 1·1 and 2·9% depending on frequency.

Introduction

Electrical impedance tomography (EIT) is a non-invasive imaging technique with applications in medicine and industry. It is based on the concept that an electrical alternating current passing through an electrically conductive object develops a voltage distribution on its surface. This voltage distribution is measured and used in a reconstruction algorithm to generate an image of the impedance distribution inside the object. In a commonly used design, the tomographic imaging system normally comprises 16 electrodes arranged symmetrically on the periphery of the subject. If a low frequency current is injected through an adjacent pair of electrodes, the resulting potential differences can be measured between all remaining adjacent pairs of electrodes. By using all possible current drive electrode pairs, a total of 13×16 different potential differences around the object can be measured. After collection of reference potential difference information, the relative resistivity distribution within the object is reconstructed using a back projection technique along the equi-potential lines [1]. A block diagram of the system is shown in figure 1.

The waveform generator is the heart of the system and has to deliver a well-defined and stable output signal. The standard approach is to use a constant sinusoidal current generator to set up the equipotentials in the subject. However, we have proposed the use of a voltage source and measurement of the resulting current for subsequent correction for the measured voltage distribution [2]. A frequency range between a few kHz and a few MHz is used in EIT for *in vivo* studies: lower frequencies might interfere with internal signals in the body, while the upper frequency limit is often set by the practical limitations of the electronic circuits used.

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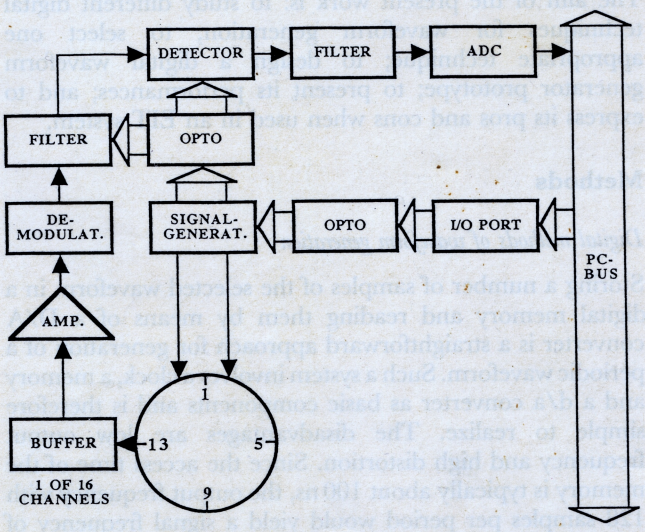

Figure 1. Block diagram of the electrical impedance tomography system with 16 electrodes evenly spaced around the subject. The system is designed to work in a semi-parallel mode and reads the resulting potential differences between adjacent electrodes more or less instantaneously. (Only one of the 16 output channels from the measurement object is shown).

However, for the present application a frequency range of 1·5–200kHz has been specified. The harmonic distortion of the generator should be as low as possible, with an acceptable value around 1%. Variation in the signal amplitude can, to some extent, be compensated for by the measuring device, but should be kept as low as possible.

The choice of method of waveform generation for use in EIT is becoming gradually more significant. This has resulted in the development of a wide variety of dedicated circuits for use in different systems.

The Wien-bridge oscillator is a good choice for many applications. An oft used version involves only one operational amplifier and some resistors and capacitors [3]. An extended version is described by Van der Walt [4]. This Wien-bridge circuit is capable of generating a 5 kHz sine wave output signal with distortion as low as 0·01%.

Another oft used signal source is the function generator. It is well established and easy to implement. These generators often comprise sine, triangular and square wave outputs and can be tuned over a large frequency range.

Digital function generators have recently been used by several authors {5, 6]. A digital waveform generator is in principle, designed around different combinations of

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memories, digital-to-analogue (D/A) converters and control logics, which enables a wide range of arbitrary waveforms to be generated. It is possible to perform fast phase-shifts, add sinusoidal waveforms at different frequencies, use modulated signals and generate accurate control signals for the demodulators, etc. Digital waveform generators enable real-time computer control of all important signal parameters, resulting in an additional flexibility of the EIT system.

The aim of the present work is: to study different digital techniques for waveform generation; to select one appropriate technique; to design a digital waveform generator prototype; to present its performances; and to express its pros and cons when used in an EIT system.

Methods

Digital methods of waveform generation

Storing a number of samples of the selected waveform in a digital memory and reading them by means of a D/A converter is a straightforward approach for generation of a periodic waveform. Such a system involves a clock, a memory and a d/a converter as basic components and is therefore simple to realize. The disadvantages are low output frequency and high distortion. Since the access time of the memory is typically about 100 ns, the output frequency with 128 samples per period would yield a signal frequency of about 80 kHz. With fewer samples, the upper frequency as well as the resulting distortion will increase. However, hybrid techniques offer generation of smooth curves without adding reconstruction filters. Four different methods are considered the basic idea of which is to add two different signals to achieve as correct a sinusoidal output as possible. The differences between the methods are the shapes of the two signals and the way in which they are generated.

Slope-plus-slope and slope-plus-pedestal techniques

In these synthesis techniques a pair of multiplying D/A converters (MDAC) are used. A triangular waveform is applied as a reference input, as discussed by Evans and Towers. A clock generator determines the frequency of the system and drives a counter (figure 2). The counter cyclically addresses two programmable read-only memories (PROM) and provides two control signals. One of these controls the output buffers preventing mismatches and variations in the PROM access times from being transmitted to the MDAC, where the efffect would be serious and result in an unpredictable distortion of the output. The other controls a reference to the phase-locked-loop (PLL). The PLL controls a voltage-controlled oscillator (VCO), which provides a triangular reference slaved to the same phase and frequency as the most significant bit (MSB) of the cyclic address.

In the slope-plus-slope technique the reference supplies the two MDACs. The phase relationship between the output from the buffers and the reference is arranged so that a flat peak top approximation of the sinewave is achieved. The linear interpolated output is formed as the sum of the two MDAC outputs. In the slope-plus-pedestal technique, one of the MDACs uses a DC level as reference so that one can use the same system merely by changing the contents of the memories.

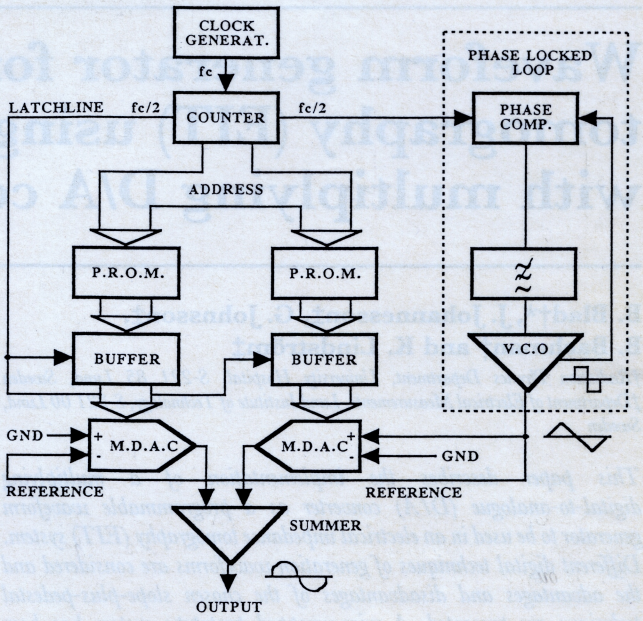

Figure 2. Block diagram of a sinusoid generator with a clock generator controlling the analogue PLL and PROM. The buffers are latched to achieve a flat peak top approximation. The two output signals from the MDACs are added and the frequency of the approximation is equal to that of the triangular reference.

These techniques give a total calculated harmonic distortion (THD) of 0·59% at 16 samples per period. At the same number of samples the staircase sine wave produces an output with a calculated THD of 11·3%. In spite of the low distortion, one of the disadvantages of these two methods is discontinuity in the signals of the channels. This a potential source of spikes in the output and will result in distortion. The other disadvantage is the PLL circuit that increases the complexity and makes it difficult to sweep the generator frequency since the centre frequency of the PLL often is determined by a resistor–capacitor combination. In figures 3 and 4 one cycle of a sinusoid using the slope-plus-slope technique and the slope-plus-pedestal technique respectively is presented.

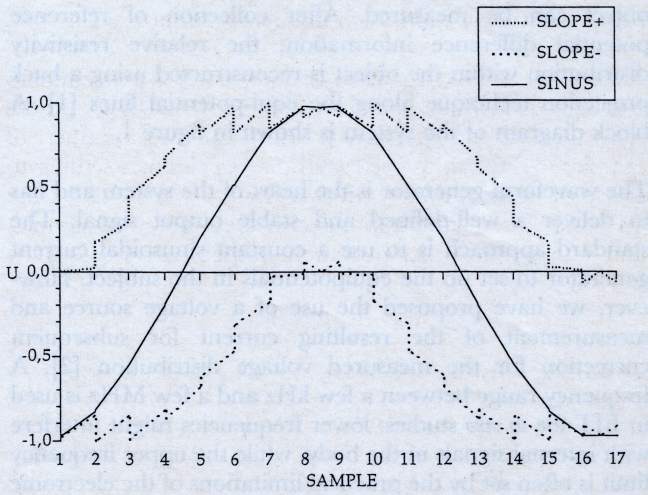

Figure 3. One cycle of a sinusoid using the slope-plus-slope technique. The two slope approximations are added to achieve a sinusoid. The voltage (U) the output from the generator is presented as function of samples.

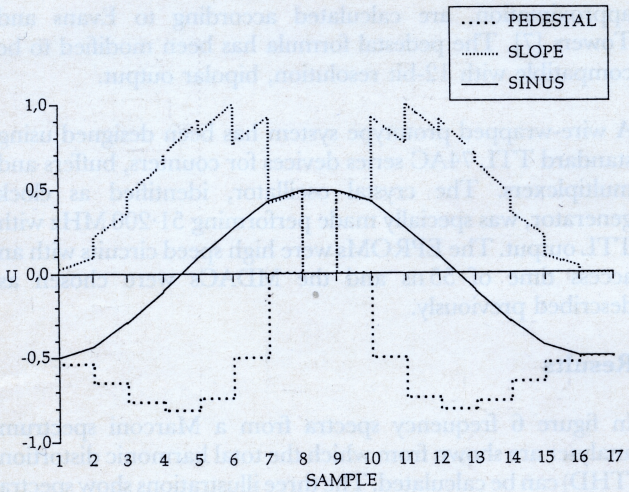

Figure 4. One cycle of a sinusoid using slope-plus-pedestal technique. The two slope approximations are added to achieve a sinusoid. The voltage (U) the output from the generator is presented as function of samples.

Other techniques

Another technique for implementing linear interpolation is the staircase-plus-sawtooth technique, described by Towers [8]. The advantage of this technique is that few circuit components are involved. The disadvantage is a potential risk of glitches, since, in practice, the two memories do not deliver their outputs simultaneously and it is difficult to achieve sufficiently fast resetting of the sawtooth reference. The triangle-plus-triangle technique offers an inherently glitch-free method of generating a sinusoidal approximation, similar to those earlier presented, but requires fewer words to generate a low distortion waveform [8].

The selected technique

After consideration of matters such as maximum output frequency and resulting circuit complexity, the slope-plus-pedestal technique was chosen for EIT applications. Although this technique has the disadvantage of possible glitches in the output signal, it is preferred to the triangle-plus-triangle technique, since the latter cannot produce low distortion, high frequency output signals.

Since the measured signals in EIT are small, it is essential to use high quality components including the MDAC. At the maximum output frequency (200 kHz) and number of samples (64) the fastest settling time, specified as settling to one least significant bit (LSB), was found to be 78 ns for the MDAC. The relationship between the number of samples and settling time for the maximum output frequency is given in table 1.

Table 1. Output frequency versus number of samples and settling time of the D/A converters.

Output frequency (kHz)	Number of samples	Settling time (ns)
200	16	313
200	32	156
200	64	78

The D/A converter used (AD 668, Analog Devices) has a settling time of 50 ns. Two of these converters generate the inputs to an amplifier, where the slope and pedestal signals are added. In order to generate eight different frequencies in the range 1·5625–200 kHz, separate timing resistors and capacitors of the PLL have to be switched by analogue multiplexers. However, such a method is often associated with temperature drift problems and it is critical that the vertices of the generated triangular wave coincide with the transaction of the MSB of the cyclic address.
An alternative approach to avoid such problems is to implement a digital version of the PLL's function. This would eliminate the drift problem, achieve simultaneous synchronizing of the system and lock the triangular wave frequency to the MSB of the cyclic address at all frequencies. However, a quantization error is introduced, and is directly added to the output. The error can be calculated where error = $1/2^n - 1$.

An 8-bit A/D converter will result in an error of 0·39%. The advantages of choosing the digital version of the PLL's function are that all phase differences between the MSB of the cyclic address and the reference are minimized and stable at all frequencies, and the stability of the reference itself is increased. It should also be noted that the risk of peak-roundings of the wave is minimmized as long as the converter is able to count up to the full-scale value and down to zero during one period of the output frequency. Different output frequencies can be controlled from a digital multiplexer

The amplitude of the output is controlled by a 4-bit digital code and thereby allows 16 different amplitudes. In order to achieve symmetrical shape of the output, both the slope and the pedestal values are scaled to fit in for every amplitude and the pedestal values are also set to correct offset. These values are then stored in EPROMs. All control signals are generated by a PC and communication is handled by the data bus.

In figure 5 one cycle of a sinusoid using the digital slope-plus-pedestal technique is shown. The values, which are stored in the EPROMs to produce the sinusoid

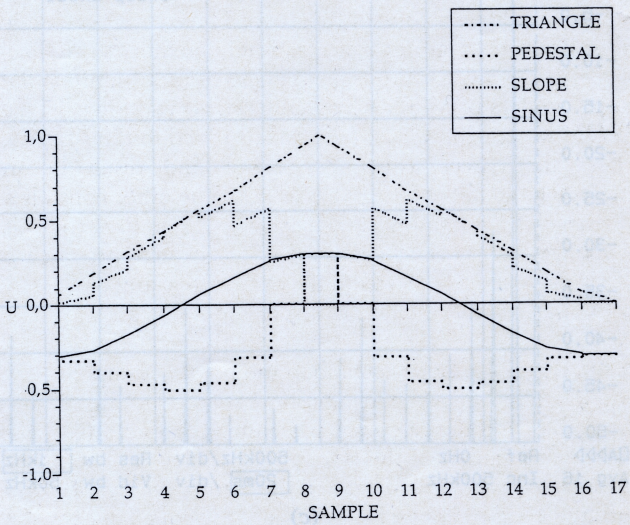

Figure 5. One cycle of a sinusoid using digital slope-plus-pedestal technique. The triangle is made by digital techniques. The voltage (U) the output from the generator is presented as function of samples.

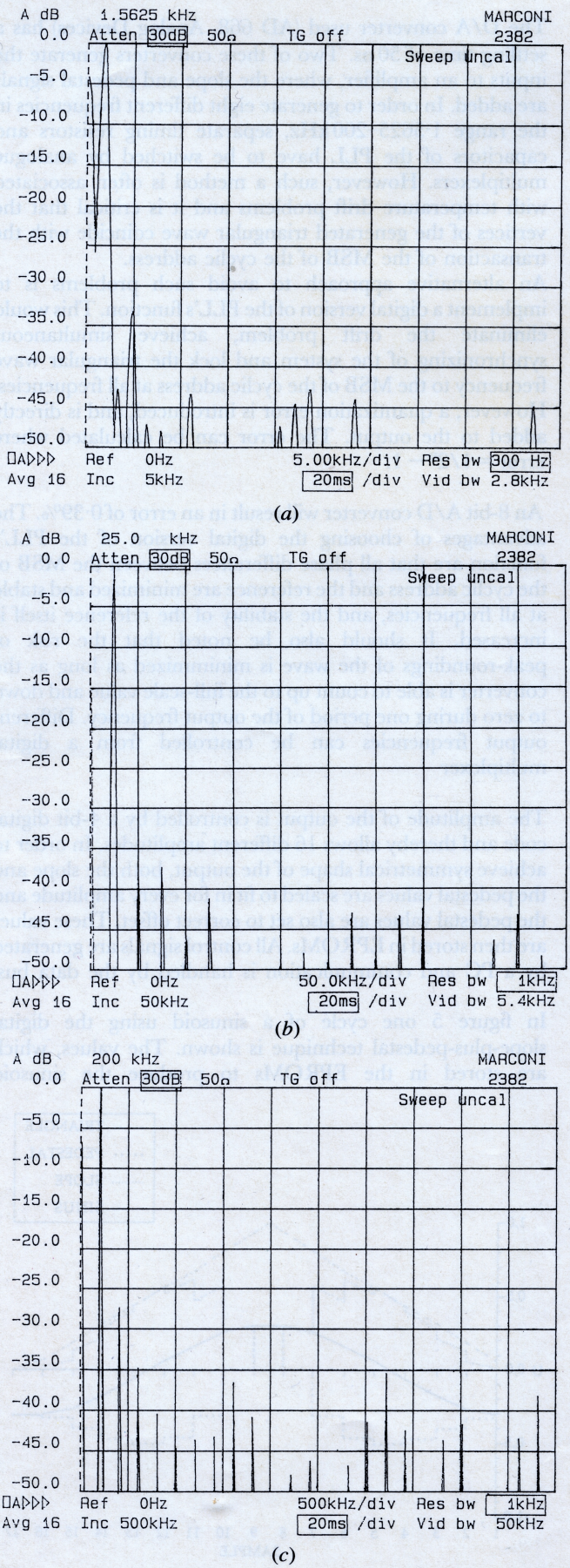

Figure 6. Measured frequency spectra for three different synthesized sinusoids: (a) 1·5625 (b) 25 and (c) 200 kHz. Note that THD increases with frequency.

approximation, are calculated according to Evans and Towers [7]. The pedestal formula has been modified to be compatible with 12-bit resolution, bipolar output.

A wire-wrapped prototype system has been designed using standard TTL 74AC series devices for counters, buffers and multiplexers. The crystal oscillator, identified as clock generator, was specially made performing 51·200 MHz with TTL output. The EPROMs were high speed circuits with an access time of 55 ns and the MDACs were chosen as described previously.

Results

In figure 6 frequency spectra from a Marconi spectrum analyser are shown from which the total harmonic distortion (THD) can be calculated. The three illustrations show spectra for 1·5625, 25 and 200 kHz respectively. The lower limit is set to 50 dB below the fundamental frequency. The second harmonic is dominant for the lowest frequency − 33 dB compared with the fundamental. In the second frequency spectrum presented the second and third harmonics yield − 37 and − 38 dB compared with the fundamental respectively. The last and highest frequency yields a larger distortion. The high distortion levels are mainly due to unoptimized practical circuit design and further improvement is therefore essential. The calculated THD values for all frequencies are presented in table 2.

These values are not acceptable compared with the theoretical values which are calculated to $< 1\%$ THD. Subsequently a new grounding system, as described by Ott [9] was introduced. This improved the system and reduced the noise levels of the outputs of the MDACs to about half of the previous system values. By inserting separate power stabilization on all the different analogue and digital printed circuit boards and in addition using signal line noise filters (EMI-FIL®) the noise levels were further reduced. The latest harmonic distortion values can be seen in table 3.

Additional reduction of the distortion can probably be accomplished if the stored values in the PROMs are refined, since the contribution of the lowest overtones are proportionally dominant

Discussion

Previous systems using the slope-plus-pedestal or the slope-plus-slope techniques [7] have been implemented with an analogue PLL, but the technique described here offers a number of advantages over the former. Using an analogue

Table 2. Total harmonic distortion of the waveform generator, measured at different frequencies.

Frequency (kHz)	1·5625	3·125	6·25	12·5	25	50	100	200
THD (%)	2·5	3·3	3·6	2·8	2·5	3·1	4·7	5·7

Table 3. Total harmonic distortion measurements at different frequencies after improvement of the waveform generator circuit.

Frequency (kHz)	1·5625	3·125	6·25	12·5	25	50	100	200
THD (%)	1·3	1·1	1·1	1·4	1·8	2·3	2·9	2·6

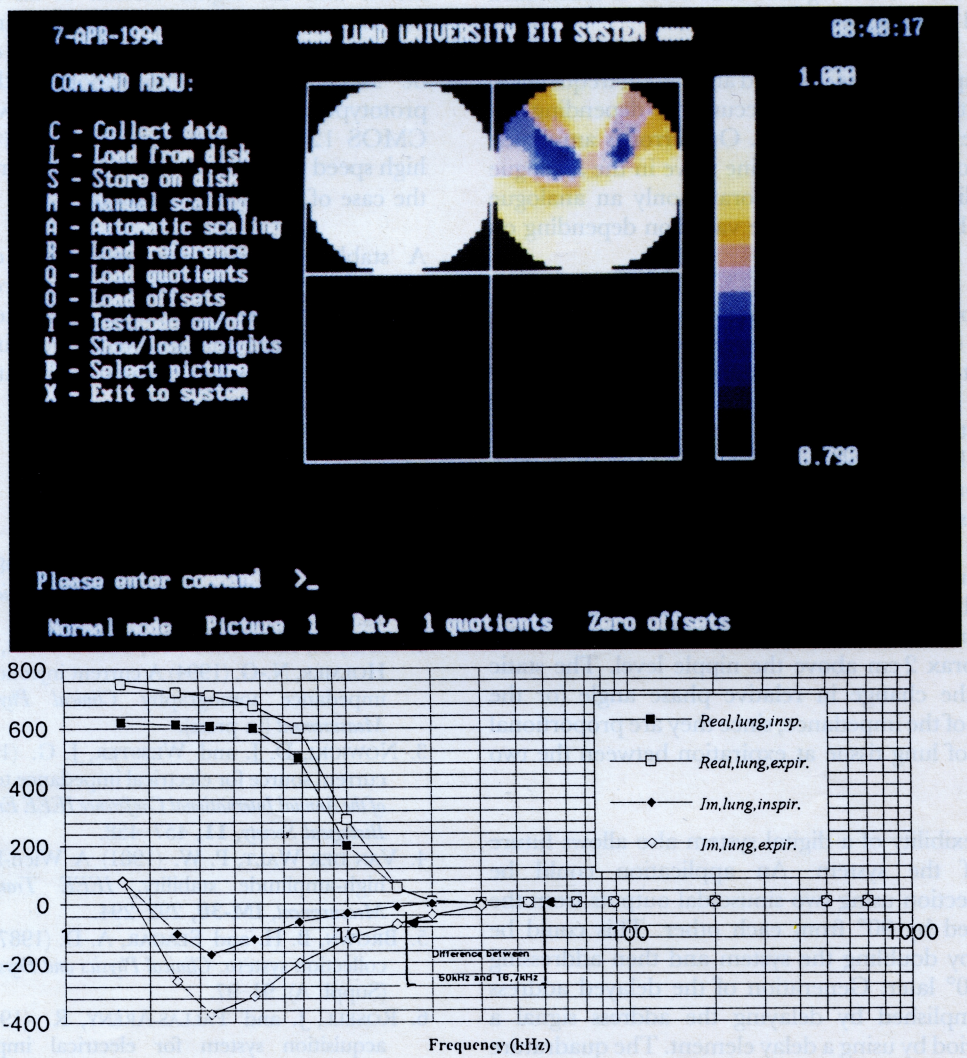

Figure 7. Imaginary associated image at 50 kHz is used as a reference and the change in reactant between 50 and 16·7 kHz is displayed at expiration. This change depends on the differences in imaginary part of the impedance in lung tissue compared to the surrounding tissue of the two frequencies (blue means bigger difference than white). This technique can probably be used for studying the extra- and intra cellular impedances of different tissues. (b) The diagram shows the impedance spectra of lung tissue at inspiration and expiration.

PLL often means circuit complexity and the frequency sweep is determined by the lock range of the PLL. Linearity of the triangular reference becomes critical when the number of samples and the word length of the samples are increased. It is also essential that the symmetry of the reference is kept stable, but with increasing frequency this often becomes difficult without stringent requirements to stabilize the VCO. Compensation for temperature drift is also a well-known problem when an analogue circuit design is used.

Our technique does not need an analogue PLL, since all the functions performed by the PLL are implemented digitally. This eliminates the above-mentioned problems and in particular, the linearity is improved. Strict lock-in on all frequencies is also achieved and is in phase, since the system frequencies control the cyclic address, the buffers and the reference. The digital generation of the reference can also be used in the triangle-plus-triangle technique and thereby offers an increased upper limit of the output frequency. This is very attractive since the output signal from this technique is, as mentioned before, glitch-free. However, the use of a quantified triangular reference will imply a quantization error. This could be kept rather small with the use of high-speed circuits and a large number of samples in the reconstruction. with 8-bit resolution the quantization error will be about 0·4%.

The waveform generator offers advantages compared with an analogue option. By this technique it is possible to produce irregular waves such as a summation of several sine waves of different frequencies. In consequence simultaneous images, containing complex impedance information can be obtained from different frequencies.

In the electrical impedance tomography system the real and the imaginary parts of the impedance seem more difficult to acquire, compared with the amplitude of the impedance. One reason for that is difficulties in generation of the two control signals, 90° apart, either to synchronous demodulators or to multipliers used for demodulation. The analogue version often uses comparators to produce these control signals. Noise in the sinusoid results in undesirable

phase shifts of the control signals. This error is minimized with the digital option.

In order to compare images collected at different frequencies, it is important to minimize inaccuracies depending on different frequencies in the system. One error is amplitude variation due to frequency of the sine wave in the analogue version. The digital design incorporates only an analogue amplifier, which reduces amplitude variation depending on frequency.

To show the consequence of this an image was obtained by EIT using our digital waveform generator. Reference data was collected at 12·6 kHz. Adjacent current injection and all the remaining voltage differences were acquired at all possible current injection electrode combinations. This gave a data set of 13×16 voltage differences used in a back projection reconstruction algorithm along the equipotential lines. Another set of data was collected at 50 kHz, and the change in the reconstructed image compared with the reference information is shown in figure 7. Sixteen silver–silver chloride electrodes (Blue sensor, P-00-A, Medicotest) were attached at equidistant distances in a ring around the thorax 2 cm above the nipple level. The static image shows the change in relative phase angle (or the imaginary part of the impedance, since they are proportional to each other) of lung tissue at expiration between the two frequencies.

The built-in flexibility of a digital system also allows future refinements of the system. An application could be quadrature detection using two sinusoidal outputs from the system separated by 90° from each other. This could be accomplished by doubling the system and then addressing one of these 90° later. Generation of the delayed address signal is accomplished by delaying the address signal a quarter of a period by using a delay element. The quadrature detection is a useful application, not only in electrical impedance tomography, but also in other modalities, such as ultrasound.

Conclusions

The technique presented uses some previously known interpolation methods in a new way. The limitation in the upper frequency range has been discussed and we have shown that the digital version of an analogue PLL can produce better results. Although the triangular reference has got a quantization error, the advantages of the technique will be useful for the interpolation methods described. A prototype has been designed, based on two high performance CMOS 12-bit MDAC, one 8-bit high speed MDAC and high speed circuit devices and its performance examined for the case of sinusoid generation.

A stable sinusoid with acceptable distortion and the possibility of creating signals to control the synchronous demodulators are advantages of this technique compared with the present analogue technique, in spite of its design complexity and upper frequency limitation (200 kHz).

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